

02-10-04

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February 9, 2004

**VIA US MAIL**

MAIL STOP DD  
Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

Re: App No. 10/624,097; "Point to Point Memory Expansion Stacking System and Method"; Docket No. 0254-094-CIP-4/CIP-1

Dear Commissioner:

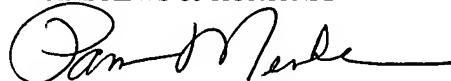
Please find enclosed for filing the following:

1. Information Disclosure Statement;
2. Form 1449 (and one duplicate copy);
3. 143 references; and
4. a return postcard for confirmation of receipt.

The Commissioner is hereby authorized to charge any fees which may be required to Deposit Account 50-0897. Please return the postcard confirming your receipt of the enclosed materials.

Yours truly,

ANDREWS & KURTH LLP

A handwritten signature of Pam Menke in black ink.

Pam Menke  
Board Certified Legal Assistant in Civil Trial Law  
Texas Board of Legal Specialization

/pm  
enclosures

AUS:553358.1

Austin

Dallas

Houston

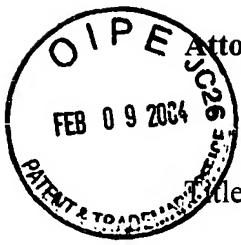
London

Los Angeles

New York

The Woodlands

Washington, DC



Attorney Docket No.: 0254-094-CIP-4/CIP1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title: Point to Point Memory Expansion System and Method

Application No.: 10/624,097

Filing Date: 07/21/2003

Inventor: James W. Cady, et al.

Assignee: Staktek Group, L.P.

Examiner: TBA

Group: 2818

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

Pursuant to the guidelines for Information Disclosure Statements, 37 C.F.R. §§ 1.97-1.98, attached hereto is PTO Form 1449 (nine sheets) with references listed for consideration by the Office.

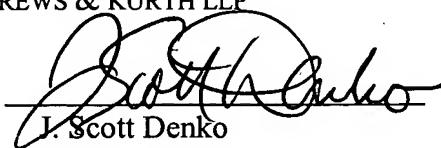
In accordance with 37 C.F.R. § 1.98(a), copies of the listed written references are being provided.

In accordance with 37 C.F.R. §§ 1.97(g)-(h), the filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made or an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b) or prior art under 35 U.S.C. §§ 102 or 103.

This Information Disclosure Statement is being filed before receipt of the first Office action, so no fee is believed to be due. The Commissioner is hereby authorized to charge any fees which may be required in connection with the filing, or to credit any overpayment to Deposit Account No. 50-0897, upon which account the undersigned has the authority to sign. **A duplicate copy of Form 1449 is enclosed.**

Respectfully submitted,

ANDREWS & KURTH LLP

By: 

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Feb. 9, 2004

Date

Form PTO-1449 (Modified)  
(Rev. 11/92)U.S. Dept. of Commerce  
Patent and Trademark OfficeINFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

(37 CFR 1.98(b))

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PATENT & TRADEMARK OFFICE

ATTY. DOCKET NO. SERIAL NO.

0254-094-CIP-4/CIP-1 10/624,097

## APPLICANT

Cady, et al

## FILING DATE

7/21/03 GROUP

2818

## U.S. PATENT DOCUMENTS

*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)
	4,763,188	8/9/1988	Johnson, Thomas	357/74		11/4/1987
	5,239,198	8/24/1993	Lin et al.	257/693		7/2/1992
	6,028,365	2/22/2000	Akram et al.	257/778		3/30/1998
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	6,265,660B1	7/24/2001	Tandy, Patrick W.	174/52.4		8/18/2000

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						Yes	No
	5-21697(A)	01/1993	Japan			Partial	
	57-31166(A)	02/19/1982	Japan			Partial	
	58-96756(A)	06/08/1983	Japan			Partial	
	58-112348(A)	07/04/1983	Japan			Partial	
	60-254762	12/1985	Japan	-	-	Partial	
	62-230027(A)	10/08/1987	Japan			Partial	
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OTHER DOCUMENTS  
(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

	Dense-Pac Microsystems, 16 Megabit High Speed CMOS SRAM DPS1MX16MKn3
	Dense-Pac Microsystems, 256 Megabyte CMOS DRAM DP3ED32MS72RW5
	Dense-Pac Microsystems, Breaking Space Barriers, 3-D Technology 1993
	Dense-Pac Microsystems, DPS512X16A3, Ceramic 512K X 16 CMOS SRAM Module
	“Design Techniques for Ball Grid Arrays,” William R. Newberry, Xynetix Design Systems, Inc.
	“Chip Scale Packaging and Redistribution,” Paul A. Magill, Glenn A. Rinne, J. Daniel Mis, Wayne C. Machon, Joseph W. Baggs, Unitive Electronics Inc.

EXAMINER

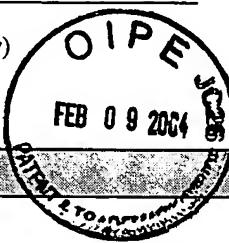
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Cady, et al	
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U.S. PATENT DOCUMENTS

*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)
	6,300,679B1	10/9/2001	Mukerji et al.	257/738		6/1/1998
	6,462,412B2	10/8/2002	Kamei et al	257/723		1/17/2001
	6,465,893B1	10/15/2002	Khandros et al.	257/777		10/19/2000
	6,486,544B1	11/26/2002	Hashimoto, Nobuaki	257/686		9/3/1999
	6,560,117B2	5/6/2003	Moon, Ow Chee	361/749		8/30/2001
	6,572,387B2	6/3/2003	Burns et al.	439/69		3/19/2002
	6,590,282B1	7/8/2003	Wang et al.	257/686		4/12/2002
	6,600,222B1	7/29/2003	Levardo, Melvin N.	257/686		7/17/2002

FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

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						Yes	No
	EP 461-639-A	12/1991	European			X	
	EP 0 298 211 A#	01/11/1989	European			X	
	EP 122-687-A	10/24/1984	European			X	
	SU 834-957	05/30/1981	Russian			Partial	

OTHER DOCUMENTS

(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

	"Alterable Interposer Block for Personalizing Stacked Module Interconnections," <i>IBM Technical Disclosure Bulletin</i> , Vol. 30, No. 8, January 8, 1988, pp. 373-374.
	IBM Preliminary 168 Pin SDRAM Registered DIMM Functional Description & Timing Diagrams
	"3D Interconnection for Ultra-Dense Multichip Modules," Christian VAL, Thomson-CSF DCS Computer Division, Thierry Lemoine, Thomson-CSF RCM Radar Countermeasures Division
	"High Density Memory Packaging Technology High Speed Imaging Applications," Dean Frew, Texas Instruments Incorporated
	Teresa Technologies, Inc. - Semiconductor Intellectual Property, Chip Scale Packaging - Website pages (3)
	"Tessera Introduces uZ™ - Ball Stacked Memory Package for Computing and Portable Electronic Products" Joyce Smaragdis, Tessera Public Relations; 2 figures that purport to be directed to the uZ™ - Ball Stacked Memory Package.

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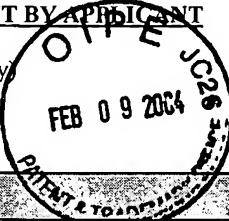
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0254-094-CIP-4/CIP-1	10/624,097
APPLICANT	
Cady, et al	
FILING DATE	GROUP
7/21/03	2818

**U.S. PATENT DOCUMENTS**

*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)
	6,620,651B2	9/16/2003	He et al.	438/113		10/23/2001
	US2002/0139577A1	10/3/2002	Miller, Charles A.	174/261		3/27/2001
	US2002/0164838A1	Nov-02	Moon et al.	438/107		6/5/2001
	US2002/0180022A1	12/5/2002	Emoto, Yoshiaki	257/686		7/19/2002
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	3,727,064	04/10/1973	Bottini	250/217		03/17/1971
	3,654,394	04/04/1972	Gordon	179/15 BL		07/08/1969
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Document Number	Date	Country	Class	Subclass	Translation	
					Yes	No

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Ron Bauer, Intel. "Stacked-CSP Delivers Flexibility, Reliability, and Space-Saving Capabilities", Spring 2002.
Tessera uZ Ball Stack Package. 4 figures that purport to be directed to the uZ - Ball Stacked Memory, 1 Page.
"Vertically-Integrated Package," Alvin Weinberg, Pacesetter, Inc. and W. Kinzy Jones, Florida International University

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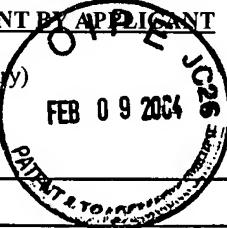
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Cady, et al

## FILING DATE

7/21/03 GROUP 2818

## U.S. PATENT DOCUMENTS

*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)
	4,103,318	07/25/1978	Schwede	361/388		05/06/1977
	4,288,841	09/08/1981	Gogal	361/414		09/20/1979
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## FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No

## OTHER DOCUMENTS

(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

	Chip Scale Review Online - An Independent Journal Dedicated to the Advancement of Chip-Scale Electronics. (Website 9 pages) Fjelstad, Joseph, Pacific Consultants L.L.C.
	Flexible Thinking: Examining the Flexible Circuit Tapes. (Website 2 pages) Fjelstad, Joseph.
	Die Products: Ideal IC Packaging for Demanding Applications - Advanced packaging that's no bigger than the die itself brings together high performance and high reliability with small size and low cost. (Website 3 pages with 2 figures) Larry Gilg and Chris Windsor. December 23, 2002.
	Flexible Printed Circuit Technology - A Versatile Interconnection Option. (Website 2 pages) Fjelstad, Joseph. December 3, 2002.

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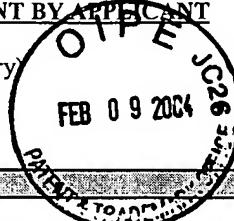
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				0254-094-CIP-4/CIP-1	10/624,097	
<u>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</u>				APPLICANT		
(Use several sheets if necessary)				Cady, et al		
(37 CFR 1.98(b))				FILING DATE	GROUP	
				7/21/03	2818	
<b>U.S. PATENT DOCUMENTS</b>						
*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)
	4,696,525	09/29/1987	Coller, et al	439/69		12/13/1985
	4,733,461	03/29/1988	Nakano	29/830		12/24/1985
	4,821,007	04/11/1989	Fields, et al	333/238		02/06/1987
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	4,956,694	09/11/1990	Eide	357/74		11/04/1988
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	5,012,323	04/30/1991	Farnworth	357/75		11/20/1989
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<b>FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION</b>						
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						Yes
						No
<b>OTHER DOCUMENTS</b> (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)						
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0254-094-CIP-4/CIP-1 10/624,097

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Cady, et al

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7/21/03 GROUP 2818

U.S. PATENT DOCUMENTS

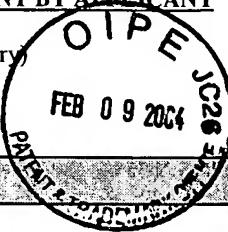
*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)
	5,041,015	08/20/1991	Travis	439/492		03/30/1990
	5,099,393	03/24/1992	Bentlage, et al	361/413		03/25/1991
	5,104,820	04/14/1992	Go, deceased, et al	437/51		06/24/1991
	5,138,430	08/11/1992	Gow, 3 <sup>rd</sup> , et al	357/70		06/06/1991
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	5,241,454	08/31/1993	Armeen, et al	361/744		01/22/1992
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	5,311,401	05/10/1994	Gates, Jr. et al	361/760		07/09/1991
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FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

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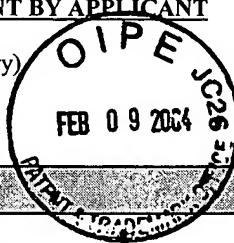
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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (Use several sheets if necessary) (37 CFR 1.98(b))						<b>APPLICANT</b> Cady, et al			
						<b>FILING DATE</b> 7/21/03		<b>GROUP</b> 2818	
<b>U.S. PATENT DOCUMENTS</b>									
*Examiner Initial	Patent Number	Issue Date	Patentee		Class	Subclass	Filing Date (if appropriate)		
	5,343,075	08/30/1994	Nishino		257/686		06/22/1992		
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	5,514,907	05/07/1996	Moshayedi		257/723		03/21/1995		
	5,523,619	06/04/1996	McAllister, et al		257/686		11/03/1993		
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	5,543,664	08/06/1996	Burns	257/787		01/20/1995
	5,561,591	10/01/1996	Burns	361/704		08/12/1994
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						Yes	No

**OTHER DOCUMENTS  
(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)**EXAMINER  DATE CONSIDERED 

\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (Modified) (Rev. 11/92)				U.S. Dept. of Commerce Patent and Trademark Office			
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (Use several sheets if necessary)  (37 CFR 1.98(b))				ATTY. DOCKET NO.		SERIAL NO.	
				0254-094-CIP-4/CIP-1		10/624,097	
				APPLICANT			
				Cady, et al			
				FILING DATE		GROUP	
				7/21/03		2818	
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<b>FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION</b>							
	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
<b>OTHER DOCUMENTS</b> (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC)							
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